SHIV NADAR
UNIVERSITY
CHENNAI

SSN School of Engineering

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Master of Technology
VLSI Design

CURRICULUM

REGULATIONS 2026

Vision of the Department

To be a nationally and globally recognized department in Electronics and Communication Engineering, offering high-quality educational programs at undergraduate, postgraduate, and doctoral levels through research and academic excellence.

Mission of the Department

We will strive towards our Vision by:

- Continued focus on academic and research excellence.
- Empowering students to become reflective professionals through curricular and co-curricular activities that instill a spirit of critical thinking, creativity, innovation, and entrepreneurial skills.
- Building partnerships with leading academic institutions and industries
- Fostering an innovative, supportive environment that encourages learning, research, and professional growth for students, faculty, and staff.

Programme Educational Objectives (PEOs)

- **PEO1**: **Professional Development**: Graduates will have a successful career in VLSI system design or associated industries or research and higher education, or as entrepreneurs.
- **PEO2**: **Attitude towards Lifelong Learning**: Graduates will have the ability and attitude to adapt the evolving technological changes.

Programme Outcomes (POs)

At the end of the programme, the graduates will achieve the following attributes:

- **PO1:** An ability to independently carry out research /investigation and development work to solve practical problems.
- **PO2:** An ability to write and present a substantial technical report/document.
- **PO3:** A sound knowledge, and design and analysis ability, in VLSI design

PEO - PO Mapping

PEO/PO	PO1	PO2	PO3
PEO1	3	2	3
PEO2	3	3	3

Programme Specific Outcomes (PSOs)

PSO1: A comprehensive understanding of fundamental and advanced concepts in VLSI Design.

PSO2: An ability to independently conduct research and development work in VLSI Design.

COURSE SUMMARY

The listed courses in the curriculum are broadly classified as per the recommendations from the UGC.

Sl. No	Broad Category of Course	Minimum Credit Requirement
1	Department Core Course (DC)	10
2	Major Core Course (MC)	30
3	Multidisciplinary Course (MD)	10
4	Open Elective (OE)	2
5	Project Dissertation (PD)	20
6	Research Internship (RI)	4
5	Skill Enhancement Course (SEC)	4
Total		**80**

The semester wise credit breakup of the Curriculum based on the above credit breakup proposed by the UGC is as follows:

Semester\Category	DC	MC	MD	OE	PD	RI	SEC	TOTAL
I	7	8	4	2	-	-	2	**23**
II	3	14	3	-	-	-	2	**22**
III	-	8	3	-	8	4	-	**23**
IV	-	-	-	-	12	-	-	**12**
Total	10	30	10	2	20	4	4	**80**

SEMESTER I

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Mathematical Foundations for VLSI Design	MD	4	60	0	0	60	120	4
2		High Level Synthesis	DC	5	45	0	30	75	150	4
3		Analog CMOS VLSI Design	DC	3	45	0	0	45	90	3
4		Digital CMOS VLSI Design	MC	5	45	0	30	75	150	4
5		Elective 1	MC	5	45	0	30	75	150	4
6		Research Methodology / IPR/Operations Research	OE	2	30	0	0	30	60	2
7		Analog IC Design with EDA Platforms	SEC	3	0	15	30	45	90	2
TOTAL				**27**	**270**	**15**	**120**	**405**	**810**	**23**

SEMESTER II

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Elective 2	MD	3	45	0	0	45	90	3
2		Design for Testability	DC	3	45	0	0	45	90	3
3		Mixed Signal CMOS VLSI Design	MC	5	45	0	30	75	150	4
4		RF CMOS VLSI Design	MC	5	45	0	30	75	150	4
5		Elective 3	MC	3	45	0	0	45	90	3
6		Elective 4	MC	3	45	0	0	45	90	3
7		DFT with System Verilog	SEC	3	0	15	30	45	90	2
TOTAL				**25**	**270**	**15**	**90**	**375**	**750**	**22**

SEMESTER III

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Multi-disciplinary OPEN Elective	MD	3	45	0	0	45	90	3
2		Elective 5	MC	5	45	0	30	75	150	4
3		Elective 6	MC	5	45	0	30	75	150	4
PRACTICALS										
4		Project/Dissertation Phase I	PD	16	0	0	240	240	480	8
5		Research Internship	RI	0	0	0	0			4
TOTAL				**29**	**135**	**0**	**300**	**435**	**870**	**23**

SEMESTER IV

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
PRACTICALS										
1		Project/Dissertation Phase II	PD	24	0	0	360	360	720	12
TOTAL				**24**	**0**	**0**	**360**	**360**	**720**	**12**

ELECTIVE 1

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Algorithms for VLSI Physical Design	MC	5	45	0	30	75	150	4
2		Scripting Languages for VLSI	MC	5	45	0	30	75	150	4
3		Semiconductor Device Modeling	MC	5	45	0	30	75	150	4

ELECTIVE 2

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Optimization Techniques for VLSI CAD	MD	3	45	0	0	45	90	3
2		Applied Mathematics for VLSI Circuits	MD	3	45	0	0	45	90	3
3		TCAD for Silicon Technologies	MD	3	45	0	0	45	90	3

ELECTIVE 3

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		System on Chip (SoC) Design	MC	3	45	0	0	45	90	3
2		Reconfigurable VLSI Architectures	MC	3	45	0	0	45	90	3
3		Neuromorphic Chip Design	MC	3	45	0	0	45	90	3

ELECTIVE 4

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		VLSI Fabricación and Packaging Technology	MC	3	45	0	0	45	90	3
2		Flexible Electronics	MC	3	45	0	0	45	90	3
3		3D ICs	MC	3	45	0	0	45	90	3

ELECTIVE 5

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Nano Scale Devices	MC	5	45	0	30	75	150	4
2		Memory Design and Testing	MC	5	45	0	30	75	150	4
3		Digitally Assisted Analog and Analog Assisted Digital IC Design	MC	5	45	0	30	75	150	4

ELECTIVE 6

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Low Power VLSI Design	MC	5	45	0	30	75	150	4
2		VLSI Signal Processing	MC	5	45	0	30	75	150	4
3		Crypto-Processor Design	MC	5	45	0	30	75	150	4

MULTI-DISCIPLINARY OPEN ELECTIVE

S. No.	COURSE CODE	COURSE TITLE	COURSE CATEGORY	CONTACT PERIODS	Teaching and Learning Scheme (per semester)					
					L	T	P	TW& SL	TH	C
1		Wireless Network-on-Chip Design	MD	3	45	0	0	45	90	3
2		CMOS Biochips	MD	3	45	0	0	45	90	3
3		Machine learning for VLSI Design	MD	3	45	0	0	45	90	3

Note: Students from M.Tech. VLSI Design must not opt for this Open Elective

L - Lecture, **T** - Tutorial, **P** - Practical, TW & SL – Term Work & Self Learning, TH – Total Hours and **C** – Credits